

RAMCHECK DDR PRO - High Speed Adapter Manual Addendum



The RAMCHECK line now extends its comprehensive support for testing the high-speed DDR DIMM modules using the new **RAMCHECK DDR Pro Adapter** (p/n INN-8668-9). We have also introduced the **RAMCHECK Plus Pro** as a combination package of the RAMCHECK and this adapter, and the **RAMCHECK DDR Pro tester**, which does not support older SDRAM technology. This manual addendum describes the operation of this adapter as well as the **DDR S.O. DIMM Converter**.

NOTE: This page is still under construction and we plan to add much more information. Please review this page whenever you are notified by our Support Department to download a new version of the firmware.

NOTE: You must have Version 2.17 or higher of the PC Communication program to support the new DDR PRO. You can download the current PC Communications program [here](#).

OPERATION

This adapter connects to RAMCHECK via the two top 90-pin and 50-pin expansion slots. Turn RAMCHECK OFF and carefully mount the adapter onto RAMCHECK expansion slots, while pressing it gradually on both sides.

CAUTION: Plug this adapter into the expansion slots only when RAMCHECK is OFF! Failure to turn RAMCHECK OFF when connecting or disconnecting the DDR PRO Adapter may result in damage to the internal PAL chips of both the RAMCHECK and the Adapter!

While the DDR Pro adapter is installed on RAMCHECK, you can test **only** the 184-pin DDR modules. To test the 168-pin DIMM modules (available on the RAMCHECK Plus Pro tester, not available on the RAMCHECK DDR Pro), the adapter must be removed. First turn the RAMCHECK OFF and carefully remove the DDR PRO adapter by gradually pulling it up on both sides, taking care not to flex the adapter's boards.

CAUTION: Please let the adapter **COOL DOWN** for at least 1 minute before attempting to remove it from RAMCHECK. Removal of the adapter while it is still hot may impair some of the soldered connections of its delicate internal parts!



RAMCHECK automatically recognizes the presence of the DDR PRO Adapter with the following initial turn-on screen:



Required RAMCHECK Firmware Version: 2.23E or later. A newer, pre-release version may be available at the [Beta Program](#) section of our download page.

DDR DIMM HANDLING

The DDR PRO Adapter supports the 184-pin DDR DIMM modules.

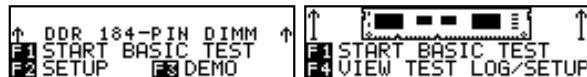
INSERTION: The DDR PRO Adapter uses a vertically mounted high quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DDR DIMM into the socket, pushing it evenly along its top. Pin 1 of the module should point to the left side (as marked on the adapter), so that the key area of the module's connector is correctly aligned with the key area in the test socket. When the DIMM is properly inserted, the ejectors will snap onto the half circle notches on each side of the module.

REMOVAL: The DIMM is easily released from the socket by pulling both ejectors sideways.

NOTE: DIMM insertion and removal should be done only when RAMCHECK is in STANDBY Mode. The RED "Module Power" LED should be OFF in STANDBY mode.

DDR DIMM TESTING

Turn RAMCHECK ON once the DDR PRO Adapter is installed. There is no need for special setup with RAMCHECK since it automatically recognizes the DDR adapter. When RAMCHECK enters the STANDBY mode, the display will prompt you to test DDR modules. Insert the DIMM module.



The DDR test procedure is initiated by pressing the F1 key and is designed to follow the regular RAMCHECK test flows. Unless you press the ESC key, **EXTENSIVE TEST** follows BASIC TEST, and **AUTO-LOOP** follows EXTENSIVE TEST.

DDR BASIC TEST

The DDR PRO allows you to set up various test parameters like the voltage, the test frequency, and the choice of a CAS Latency. The following screen previews the BASIC TEST, showing a user-selected voltage setup of 2.85V.

```
BASIC TEST 00000000
BYTES: B1 ***** B8
00:04.9 466MHZ UBF%
128Mx64 2.85V CL2.5 B1/2
```

At the start of BASIC TEST, RAMCHECK provides power and proper initialization sequence (involving control and clock lines) to the DDR module. A large variety of quick wiring tests are conducted, the module structure and frequency is determined, and the memory array tests begin. Since the wiring and structure tests are extremely fast, their results are logged in the Test Log and reported after the end of BASIC TEST, unless an error is encountered.

Before discussing the wiring and structure test results, let us review the two main phases of the BASIC TEST, the memory array tests at two different CAS Latencies. By default, RAMCHECK uses CL=2 for the first test for modules below 400MHz, and CL=3 for modules running at 400MHz or higher. The second array test is set at CL=2.5 by default. You can use setup in the **Change-on-the-Fly feature** to control the CL setting. These two array tests take the bulk of the time of the BASIC TEST.

First Memory Array Test

In its default setup, RAMCHECK selects CL=2 for modules that run below 400MHz and CL=3 for modules running at 400MHz or above. The following screens show the information provided during the first main phase of the BASIC TEST with a typical PC3200 module which defaults to CL=3:

```
BASIC TEST 55555555
BYTES: B1 XXXXXXXX B8
00:01.8 400MHZ UBF%
64Mx64 DDR CL3 B1/0

BASIC TEST AAAAAAAA
BYTES: B1 IXXXXXXXX B8
00:11.6 400MHZ UBF%
64Mx64 2.60V CL3 B1/0
```

In this example, a 64Mx64 Unbuffered (marked UBF) module is tested at CL=3 at 400MHz. The entire memory array is written and verified twice to catch most "memory cell stuck" problems. The marker to the right of the UBF message indicates that the test is set at STTL 2.5V. However, the actual voltage is automatically adjusted to 2.60V for modules running at 400MHz (2.70V for faster modules). You can use setup or change-on-the-fly to set up your own fixed voltage selection. The two screens alternate during the test so that you can see the test voltage.

The "B1/0" marker at the bottom right corner is the "section under test" indicator, which has been modified for DDR devices. With DDR devices, each chip has four internal banks, which are selected by the BA1 and BA0 bank address lines. The module itself may have one or two main banks which are selected by S0 and S1 control lines. In this example, "B1/0" indicates that the section under test is the module's first main bank (also known as rank) and the internal chips bank 0. If the marker was "B1/1", it would indicate main bank 1 and internal chips bank 1. A "B2/3" marker indicates the second main bank (rank #2) and internal chips bank 3. Similarly, "B1/2" would indicate main bank 1 and internal chips bank 2, and so on. Modules with only one main bank will scan "B1/0"->"B1/1"-> ... ->"B1/3", before switching to the next test pattern. Modules with two main banks will scan "B1/0"-> ... ->"B1/3"->"B2/0"->...->"B2/3" for each test pattern.

Some modules cannot run at CL=3, or are setup by the user to test at CL=2. The following screen shows the information provided during an array test at CL=2:

```
BASIC TEST 55555555
BYTES: B1 XXXXXXXX B8
00:02.6 400MHZ UBF%
64Mx64 DDR CL2 B1/0
```

In this example, a 64Mx64 Unbuffered (marked UBF) module is tested at CL=2 at 400MHz.

Please note that a 400MHz module may legitimately drop in speed during the more stringent CL2 CAS LATENCY array test. Similarly, a 266Mhz module may drop to 233Mhz or 200Mhz (a 333MHz module to 300Mhz or 266MHz) during the CL2 array test.

333MHz modules currently default to CL=2 for the first array test. If you see unexplained speed drifts, try to select "Fixed CL=3->CL=2.5", as described in the Change-on-the-Fly section below.

Second Memory Array Test

After the completion of the first memory array test at CL=2, the second memory array test at CL=2.5 is conducted.

```
BASIC TEST 00000000
BYTES: B1 ***** B3
00:04.9 466MHZ UB%
128Mx64 2.85V CL2.5 B1/2
```

In this example (using a different module for the screen capture), a 128Mx64 Unbuffered module is tested at 466MHz and at CL=2.5. If testing Registered modules, the screen will look like this:

```
BASIC TEST 00000000
BYTES: B1 ***** B3
00:08.1 333MHZ REG%
32Mx72 2.50V CL2.5 B2/2
```

Registered modules are marked by the "REG" reversed message. In the above screen, a 32Mx72 Registered module is set up at 333Mhz. Please note that the test voltage defaults to 2.50V at such frequency.

Wiring tests at the start of the Basic Test

At the start of the Basic Test, RAMCHECK performs a large number of wiring tests to verify that data lines, address lines and control lines are properly wired and function.

```
at CL=2 :
DATA WIRING - PASS
ADD. WIRING - PASS
TEST AT SSTL 2.5V
```

If no wiring problems are detected, the above screen is written into the Test Log. In the event of errors, RAMCHECK stops the test and provides error indication as well as detailed information regarding the pin connection associated with the detected error. Error report styles are similar to other RAMCHECK error reports for SDRAM and EDO/FPM devices. The following screens provide some examples:

```
DATA LINES STUCK:
CONTINUE END Est
P12=D8 at 0
ERROR 1 OF 1
```

The above screen shows data line D8 (connector pin-12) stuck at logic '0'.

```
CONT. LINES STUCK:
CONTINUE END Est
P63=-WE at 1
ERROR 1 OF 1
```

The above screen shows control line -WE (connector pin-63) stuck at logic '1'.

```
ADD. ERROR: 8 OF 9
F1 CONTINUE END Est
P125=A6 ROW
E1-NIBBLES: 00000303
```

This address error example indicates an error in row address line A6 (connector pin 125) which affect some portion of the individual chips of the module. Since all address lines multiplex both rows and columns, an address error may affect ROW, COL (column) or ROW+COL. The bottom line further shows which data bits in the current bank are affected by the detected error. This allows an advanced user (e.g. a memory technician who can repair the module) to identify individual defective chips on the module. All DQ lines are divided into 4-bit groups called NIBBLES, and the hex number indicate which nibbles are affected by the address errors. In the above example, the nibbles code ...0303 is translated to ...01100000011, indicating problems in nibbles 0,1,8 and 9.

Change-On-The-Fly for the Basic Test

RAMCHECK provides a rich sets of parameters that can be changed during the BASIC TEST. We distinguish the Change-On-The-Fly setup which affects ONLY the current test from the "permanent" Setup which controls the test parameters, unless changed by the user. For example, if you setup the frequency to 400MHz, then all tests will be fixed at 400MHz. If you run BASIC TEST and use the Change-On-The-Fly to set the frequency to 400MHz, then the current test will run at 400Mhz but subsequent tests will run at the regular default frequencies (or "permanent" setup frequencies). To reach the Setup menu, you press F2 during Standby mode. To activate the Change-On-The-Fly, you must first start BASIC TEST and then press F2. The following main menu will appear:

```
CHANGE-ON-THE-FLY:
F1 FREQUENCY Est RETURN
F2 VOLTAGE F3 MORE
F4 REFRESH F5 CL SETUP
```

Any change done via the Change-On-The-Fly menu is relevant during the current test. Permanent setup changes can be done via the regular Setup menu, which is activated by pressing F2 during STANDBY.

Expanded Change-On-The-Fly can be used to set up the Frequency, the Voltage, the CAS LATENCY and the Refresh rate only for the current test. Following the test, it returns to the current setup parameters.

```
CHANGE-ON-THE-FLY:
CAS LATENCY SETUP
F1 ENTER ABORT Est
← AUTO CL2/3 -> CL2.5 →
```

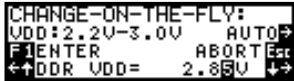
The DDR PRO allows you to set up the CAS LATENCY. This screen shows our default setup which allows the test program to selected CL=3 or CL=2 for the first array test (based on module's speed) and CL=2.5 during each test phase.

```
CHANGE-ON-THE-FLY:
CAS LATENCY SETUP
F1 ENTER ABORT Est
← CL2.5 ONLY →
```

In this example, the CAS LATENCY was fixed to CL=2.5 throughout the tests. All our CAS Latency optional selections are listed in the following table:

AUTO CL2/3->CL2.5	default setup
Fixed CL=2 -> CL=2.5	Forces the first test to start at CL=2 and the second at CL=2.5
Fixed CL=3 -> CL=2.5	Forces the first test to start at CL=3 and the second at CL=2.5
CL2 ONLY	All tests are done at CL2
CL2.5 ONLY	All tests are done at CL2.5
CL3 ONLY	All tests are done at CL3

VOLTAGE SETUP



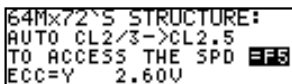
The new DDR PRO VDD Voltage setup allows the user to change on-the-fly the test voltage in the range 2.2V-3.0V. When set to AUTO, RAMCHECK automatically tests the module at 2.5V/2.7V.

Basic Test Results

The following screen shows the first summary screen following a successful Basic Test with another module:

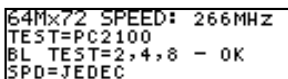


In this example, a DDR 512MB module, organized as 64Mx64 was tested at 266MHz. The module was of the Unbuffered type (UBF message), tested at 2.5V (like all DDR devices), and it uses 3 differential clock pairs.

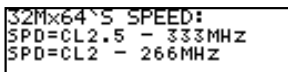


RAMCHECK Basic Test provides several screens for test results. The third structure screen shown here includes some of the new features of the DDR PRO, including the CAS LATENCY and the voltage setup.

During the Basic Test, RAMCHECK tests the operation of the three Burst Length available in DDR devices - 2, 4, and 8. Unlike older SDRAM, new DDR devices do not support Full Page Burst. The following screen shows a summary screen indicating that BL (Burst Length) was tested OK:



During the Basic Test, RAMCHECK interrogates the SPD of the module to read the maximum declared frequency at CAS LATENCY (CL) 2 and 2.5:



The above example shows the reading from a typical PC2700/PC333 module. Such a module can reach 333MHz operation only in the slower CL2 mode.

```
128Mx64'S STRUCTURE:
CL3 ONLY
TO ACCESS THE SPD F5
ECC=N 2.5/2.7V AUTO
```

Here is another example where the CAS LATENCY was set at CL3 ONLY and the voltage left at automatic mode (2.5V for modules running up to 333MHz, 2.6 or 2.7V for higher speed modules).

RAMCHECK Test Log

The RAMCHECK Test Log allows you to review all the test results in one continuous scrolling display. You can view the test even after the test ends (but before you start a new test) by pressing F3 from Standby and selecting Test Log with F1. **The Test Log is one of RAMCHECK's most powerful features.** When used with the [PC Communications](#) program, the test log can be printed and saved into convenient log files.

The following screens shows you some of the new features of the DDR PRO adapter as seen in the Test Log.

```
at CL=2.5 ->
VOLTAGE OVERRIDE:
TEST AT SSTL 2.75V
BASIC TEST ->
```

RAMCHECK's built in test log shows the actual voltage of the test.

```
ECC=N
CAS LAT. OVERRIDE:
CL3 ONLY
BASIC TEST ->
```

CAS LATENCY override is shown in the Test Log. In this example, the module is tested at CL=3 only. In the automatic (default) mode, the CAS LATENCY is changed between CL=2 and CL=2.5

```
SPD=PC3200
ARRAY TEST @CL2->
400MHZ
ARRAY TEST - OK
```

This screen shows the speed to be 400MHz during the CL2 test array portion of the test. **Please note that a 400MHz module may legitimately drop in speed during the more stringent CL2 CAS LATENCY array test..**

```
ARRAY TEST @CL2.5->
ARRAY TEST - OK
SPEED TEST RESULT:
TEST=PC3200
```

This screen shows the second array test portion of BASIC TEST, which is run at CL2.5. User can also select CL2 or CL3 or CL2.5 ONLY test.

Some 400MHz modules do not support CL=3 testing. The automatic BASIC TEST will substitute CL=2 instead for the first array test, and the following message will appear in the test log, indicating that CL=3 is not supported by the tested module.

```
CONNECTOR WIRING-OK
DATA WIRING - PASS
ADD. WIRING - PASS
CANNOT RUN @CL3
```

Module's use of DQS and DM control lines

DDR memory devices use data read/write strobe signals (DQS) as well as Data Mask (DM) signals for masking write activity on the selected chip. The DQS line controls the transfer of data from and to the memory device. When the DM signal is set high, the attached DDR device will not accept data which is written to it, that is, the written data is masked out from changing the memory device contents. The 184-pin connector includes either 9 DQS lines and 9 DM lines or only 18 DQS lines.

Most DDR modules are made of x8 type DDR chips and they are wired to use 9/8 DQS lines (9 for x72 ECC DIMMs, only 8 for x64 DIMMs). They also use 9/8 DM lines. Such modules are identified in RAMCHECK's Test Log with the line "DQS:08..0 DM:08..0" as depicted in the following screen:

```
BANKS: 1
-S:0
DQS:08..0 DM:08..0
SPD=JEDEC
```

Some Registered modules which are made of x4 type DDR chips are wired to 18/16 DQS lines (18 for x72 ECC DIMMs, only 16 for x64 DIMMs). The DM control line of the DDR chips of such modules are disabled by a fixed connection to ground. Such modules are identified in RAMCHECK's Test Log with the line "DQS:17..0" as shown in the following screen:

```
BANKS: 1
-S:0
DQS:17..0
SPD=JEDEC
```

Some examples for modules with 18 DQS control lines include Samsung (p/n M383L6420DTS) and Micron Technology (p/n MT18VDDT3272G).

DDR Parameters Setup

You can permanently change test parameters using RAMCHECK Setup Menu. You reach Setup by pressing F2 from Standby mode. Press F1 to select Parameter Setup. Setup parameter menus are similar to the Change-On-The-Fly menus discussed above. The following screen shows the DDR Voltage Setup:

```
SETUP PARAMETERS
VDD:2.2V-3.0V
F1 ENTER          ABORT Esc
←DDR VDD=        AUTO →
```

Unlike the CHANGE-ON-THE-FLY above where the new voltage setup is effective for one test, you can use the Setup Parameters to change the test voltage parameters for all tests.

DDR EXTENSIVE TEST

The EXTENSIVE TEST for DDR is similar to our regular SDRAM test. Currently, the following test phases are performed:

- Voltage Cycling
- Voltage Bounce
- March Up/Down
- Chip Heat
- Final Test

As there many R&D development efforts ongoing with the DDR PRO, we plan to add additional tests and to modify and improve the existing ones with future firmware versions.

As of this writing, we have several compatibility issues with some good modules that we are working to resolve.

Voltage Cycling

```
VOLTAGE CYCL CCCCCCCC  
BYTES: B1 ***** B8  
00:05.1 400MHZ  
64Mx72 2.40V [L3] B1/1
```

During Voltage Cycling, the program cycles the test voltage while running various memory tests. Some frequency drifts are normal for this test, as the module is periodically run at its lower voltage margin. The test can be skipped by pressing F1, or run again by pressing F2.

Voltage Bounce

```
VOLTAGE BOUNCE  
READ 55555555  
00:06.5 400MHZ  
64Mx64 2.50V [L3] B1/1
```

During Voltage Bounce, data is written to the module at a certain voltage and then read at a different voltage. Some frequency drifts are normal for this test, as the module is periodically run at its lower voltage margin. The test can be skipped by pressing F1, or run again by pressing F2.

March Up/Down Test

```
MARCH UP/DOWN  
MARCH UP AAAAAAAA  
00:28.6 400MHZ  
64Mx64 2.75V [L2.5] B1/0
```

During March Up/Down, the program attempts to catch cell interference errors. The test can be skipped by pressing F1, or run again by pressing F2.

Chip Heat Mode

```
CHIP-HEAT MODE  
1.12A  
01:01.5 400MHZ  
64Mx64 2.75V [L2.5]
```

During Chip-Heat Mode, we are using our proprietary technology to heat up the module, in preparation for the final test of Extensive Test. This mode can be skipped by pressing F1, or run again by pressing F2.

Final Test

```
FINAL TEST FFFFFFFF  
BYTES: B1 ***** B8  
02:04.6 400MHZ [UB] 4%  
64Mx64 DDR [L2.5] B1/0
```

The Final Test during Extensive Test is very similar to Basic Test. It incorporates the same two array tests. Typically, at this stage, the module has been heated up during Extensive Test and the Chip Heat Mode. This test can be repeated by pressing F2.

AUTO-LOOP TEST

The AUTO-LOOP test uses changing patterns to burn-in the module and to detect cell

interferences.

```
AUTO-LOOP 3C3C3C3C
LOOP#16 B1/1
00:00:44.0 400MHZ
64Mx64 2.40V CL3 DDR
```

The AUTO-LOOP screen indicates the current loop number and the first data of the current complex pattern. Note that each complex pattern includes an 8x72 bit array, so that the "3c3c3c3c" hex marker is just the first 32 bits of the first 64/72 bit extended word.

The screen also shows the voltage, the CL setup and current portion of the module that is being tested ("B1/1" means chip bank 1 of rank 1). Unless you have selected CL2 ONLY, CL2.5 ONLY, or CL3 ONLY, the program automatically changes the CL setup every few loops. Similarly, unless you have setup a fixed voltage, the test voltages changes every few loops. You can skip loops using F1, cycle the voltage using F2, or cycle the CL setup using F5.

```
AUTO-LOOP 0F0F0F0F
SELF REF/COOL DOWN...
00:21:36.7 400MHZ
64Mx64 2.80V CL2 DDR
```

During AUTO-LOOP, the program automatically cools down the tested module every 16 loops, so that module's operation is checked with a changing temperature gradient. Other functions like self refresh or cke controlled power down mode are exercised during the cool down period.

RAMCHECK DDR S.O. DIMM CONVERTER

The DDR **S.O. DIMM Converter** (p/n INN-8668-6-1) allows testing of 200-pin DDR S.O. DIMM modules on the DDR-184 pin adapter (p/n INN-8668-6).



The converter is made in the shape of a standard 184-pin DIMM module, but without the center key. It has special electronics for RAMCHECK's auto-detection, and it is designed for low noise and short signal connections.

OPERATION

Place the converter on a flat surface that is covered with a proper anti-static sheet. Insert the 200-pin SO DIMM into socket J2, making sure that the module's pin-1 is facing left. Socket J2 is similar to the standard laptop sockets, and it has metal latch to insure proper retention of the module in place. We have selected the AMP gold plated sockets as the best available in the market. Once inserted, the module surface locks in parallel to the converter board, with the module's front side aligning with the converter's front side.

Insert the converter into the DDR adapter's 184-pin test socket as if it was a regular DDR

module, making sure that pin-1 faces left. Press F1 to start the test, which generally follows the regular DDR test flow as outlined above.

At the end of the test (RED power LED must be off), remove the converter and place it on the protected flat surface for removal of the tested SODIMM module.

The converter is auto detected, and RAMCHECK's standby message should continue to indicate a 200-pin SODIMM until a regular 184-pin DDR module is tested.

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